REMARKS/ARGUMENTS

Claims 1 and 11 are amended. Claims 21-26 are added, and no claims are canceled. Thus, after entry of this amendment, claim 1-26 will be pending. Applicants submit no new matter has been added and request examination of the pending claims.

Claim Objections

Claims 15 and 16 are objected to because "the first function" and "the second function need to be clarified. The term "first function" has been changed to the term "user function," and the term "second function" has been changed to the term "first set of decomposed functions." Accordingly, Applicants respectfully request withdrawal of this objection.

Rejection under 35 USC § 103, Kaviani in view of Wallace or Vemuri

Claims l- 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaviani (US Patent No. 6,480,023) and further in view of Wallace (US Patent No. 6360352) or Vemuri et al., "BDD-Based Logic Synthesis for LUT-Based FPGAs", ACM Transactions on Design Automation of Electronic systems, Vol. 7, No.4, Oct. 2002, Pages 501 -525.

Claims 1-10

Claim 1 is allowable over the cited references, either alone or in combination, as those references fail to teach or suggest all the elements of claim 1. For example, claim 1 recites:

> *providing a plurality of logic blocks, each configurable to operate as any one of the following:*
>
> *one N-input lookup table wherein N is an integer; and*
>
> *at least two lookup tables, each having less than N inputs, such that the logic block has more outputs than when the logic block operates as the one N-input lookup table;*
>
> *based on an amount of variables input to the user function, determining a set of available lookup table configurations that potentially implement the user function, wherein a lookup table configuration specifies the number of the lookup tables and the number of inputs for each logic block;*

In Kaviani, each of the slices 510 (logic blocks) are made of two lookup tables (LUTs) that each have four inputs. *See Kaviani*, Figure 5 and other Figures. The slices are not

configurable to provide different LUT configurations. For example, Kaviani does not show a slice that can be configured to be either a two 4-input LUTs or a 5-input LUT. Thus, Kaviani does not teach or describe providing a logic block configurable to operate either as one N-input LUT or two LUTs having less than N inputs, as recited in claim 1.

As Kaviani does not mention different configurations for a logic block, Kaviani also does not teach or suggest determining available configurations that potentially implement the user function, as recited in claim 1.

Wallace's discussion of LUTs and FPGAs is limited to creating a netlist from a circuit, which may contain a LUT. *See Wallace*, column 8, lines 8-19 and column 14, lines 11-23. Wallace does not describe any type of configuration of a LUT or of a logic block configurable to operate as different types of LUTs, as recited in claim 1. Thus, Wallace also does not teach or suggest configurable logic blocks or determining LUT configurations, as recited in claim 1.

In Vemuri, the target technology is k-input LUTs for the technology-independent logic optimization and decomposition phase. *See Vemuri*, page 503 lines 13-15. All of the LUTs are of the same size. *See Vemuri,* Figure 5. In contrast, claim 1 recites providing a logic block configurable to operate as an N-input lookup table and at least two lookup tables with less than N inputs.

Also, Vemuri determines all of the possible cuts with k or less variables. *See Vemuri*, page 510 lines 27-33. Thus, Vemuri does not determine a set of available configurations that are available for a particular programmable circuit, as recited in claim 1.

For at least the reasons stated above, Applicant submits that claim 1 and its dependent claims 2-10 are allowable over the cited references.

Claims 11-26

Applicants submit that independent claims 11 and 21 should be allowable for at least this same rationale. Claims 12-20 depend from claim 11, and claims 22-25 depend from claim 21 and thus derive patentability at least therefrom.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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